Integrated Distributed Amplifier with Passive-Free Input Driver

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Abstract — **High efficiency amplifier operation (class-D, E and S) conceptually approaches an ideal switched transistor model. Driver signals are of sufficient level to ensure that the devices are saturated and cut off during the proper parts of the RF cycle. Conventional sine wave input signals are generated with lower efficiency cascaded power gain stages. Deep sub-micron CMOS technology and improved power device input terminal parameters, have created a novel opportunity for a new switching signal driver design approach. This can be extended to distributed power amplifier application to replace the passive lumped transmission line input network with an integrated active solution.**

I. INTRODUCTION

Distributed amplifiers have been used in many broadband small signal applications since their invention in 1935 by Percival. [1] Recent interest in all-band software defined radios (SDR) resulted in distributed amplifiers with very broadband performance and high efficiency. Narrow bandwidth limitations of resonant impedance matching of device inputs and output shunt capacitance, is overcome by distributing this capacitance in several smaller devices built into a lumped transmission line network. These lumped network sections between distributed devices are designed to provide equal phase shift or time delay allowing inphase signal combining at the device output nodes. Typically, device input capacitance dominates that of the output capacitance limiting the frequency response to the that of the lumped input network implementation. High frequency performance of deep sub-micron CMOS technology provides an alternative very wideband distributed amplifier input network. An input network with harmonic rich electronically delayed switching signals, is integrated in 0.13um CMOS technology. These are AC coupled directly into the InGaP HBT base terminals of a four section 1.5 watt final stage distributed power amplifier.

II. POWER AMPLIFIER BLOCK DIAGRAM

GSM enjoys the highest number of users across the wide world of wireless cellular technology. Since this is a constant envelope or a phase modulated physical layer application, we focused on a polar network to simplify extending this work to linear signal processing. A distributed amplifier provides a broadband solution to build a polar transmitter system on.

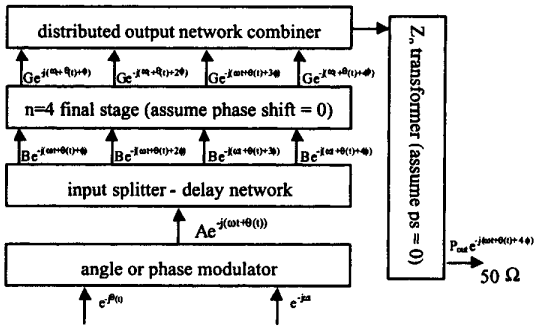

Fig. 1, constant envelope modulated distributed power amplifier transmitter system with integrated delay driver network.

This paper reduces the transmitter to five blocks see Fig. 1; input modulated signal, active delay splitter network, distributed section final device, lumped transmission line output network combiner, and broadband output impedance transformer. The input phase modulated signal is assumed to be a two state voltage with 50% average duty cycle waveform at the carrier frequency. This signal source is split into four phase or time delayed versions of the original switching signal. These are buffered with complementary MOS device inverters to drive the base or base terminal capacitance of the distributed amplifier final devices. A lumped constant-k low pass output network is designed for efficient forward power transfer at the fundamental and for harmonic termination, using the virtual impedance concept[2]. This is constrained by the practical limits of output load impedance (Eq 1) and each output network section characteristic impedance (Eq 2)[3].

$$Z_{out} \cong V_{dd}^{\ 2} / (2 * P_{out}) \quad (1)$$

Where Z_{out} is the output terminal load impedance assumed to be real, V_{dd} is the DC supply voltage (5 volts) coupled to each of the distributed device collector or drain terminals,

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and P_{out} is the desired output power at the fundamental frequency of operation.

$$Z_n = N * Z_{out} / n \qquad (2)$$

Here n is the distributed section number between 1 and N, the maximum number of sections, and Z_n is the output section characteristic impedance.

III. INTEGRATED CMOS INPUT DELAY SPLITTER DRIVER

The integrated input network is a set of series digital inverters configured as non-inverting buffers as shown in Fig. 2. Delay tuning is implemented by varying the inverter current with a gate voltage adjustment applied in common to all delay buffers. Output loading on the delay inverter pairs is buffered with an additional inverter buffer pair. This buffer stage is scaled to ensure sufficient signal to drive a load of C=5pF representing each of the distributed section final device base or gate terminal capacitance.

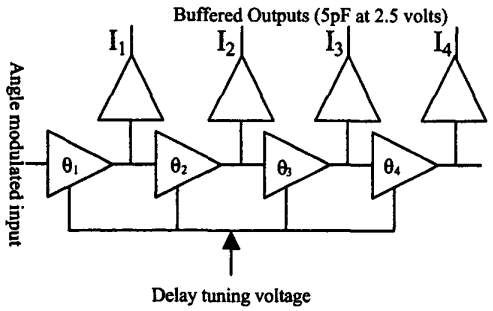


Fig. 2. Integrated digital delay and splitter implemented in CMOS 0.13um deep sub-micron technology.

Power added efficiency associated with a digital input network is estimated using the capacitance charging energy relationship.

$$P = C V^2 F / 2 \qquad (3)$$

Which is equal to 15.6 mW for 5pF at 1GHz for a total of 62.5 mW assuming n=4 distributed final device. Unlike a resonant network where the energy stored in the reactance is recycled, it is dissipated with a digital two state signal. This may be an opportunity to develop a digital signal processing with recycled energy storage. However, lowering the voltage swing from the 2.5 volts associated with FET devices to 0.5 volts of a bipolar HBT device, reduces the composite driver dissipation to 625 uW.

Motorola's 0.15um gate length deep sub-micron CMOS technology was used to integrate the input delay network, see Fig.3. Eight delay-offset outputs are provided with separate internal (1.5 volt) and external driver (2.5 volt)

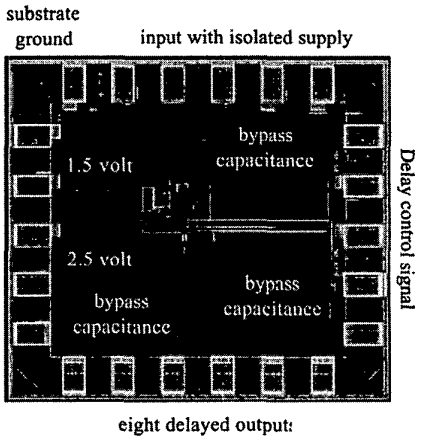


Fig. 3. Motorola's 0.15um deep sub-micron technology used to integrate a distributed power amplifier input delay network. ~700um squared

supplies. To improve noise and spurious performance an isolated supply is used with internal bypass capacitance decoupling. The 700um square integrated circuit requires no additional external components.

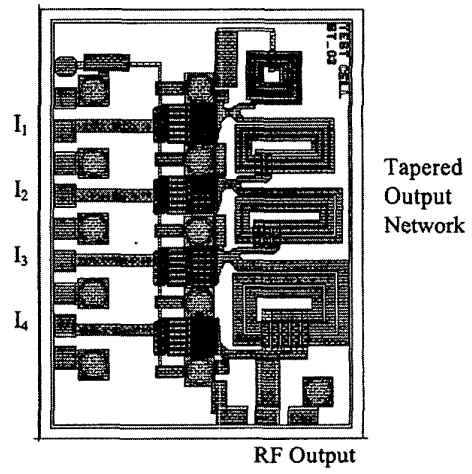


Fig. 4. Motorola's InGaP HBT technology was used to integrate 4 section single stage distributed power amplifier. ~1.8mm squared

IV. DISTRIBUTED OUTPUT STAGE

The distributed output stage is a four section single stage structure designed using virtual impedance techniques for high efficiency. It is intended for broadband wireless applications from 300 MHz to 2 GHz. It delivers 1.5 watts into 50 ohms via an output transformer/bias network.

V. PERFORMANCE

The virtual impedance of the 1 GHz fundamental, along with that of the second, third and fourth harmonics of the input signal are plotted as seen at each transistor collector node for the single ended case. The top plot in Fig. 5 shows the virtual impedance for each frequency component at the collector of the first device. The next three plots represent the activity at the remaining collectors approaching the output node. The bottom plot displays efficiency at the combined output node, which is also the last collector. It should be noted that the collector efficiency here is more then 10 percent higher then a similar amplifier with a conventional input structure driven by sine wave input waveforms. It can be seen that where the harmonic terminations are poor, especially for the second harmonic, the efficiency suffers. Furthermore, an initially well-behaved fundamental virtual impedance becomes effected by the poor harmonic terminations as it travels down the output network. At the fourth and final device, the fundamental virtual impedance is higher then optimal, yet the total efficiency is still good in the regions where most of the harmonics are well terminated.

A complete block diagram of the test fixture is shown in Figure 6. The unit will support differential or single ended distributed power amplifier operation. The input drive signal applied from the 50 Ohm source is 7.2 mW which will be reduced somewhat in higher impedance systems. Use of a differential system will help to increase the system output impedance and reduce balun transformation ratio. In addition, even order harmonic rejection is improved. This additional harmonic rejection is considered important in realizing the practical bandwidth potential of a distributed amplifier with respect to its application in telecommunications products.

VI. CONCLUSION

A novel distributed amplifier configuration with no passive slow wave structure on the input has been designed. A CMOS digital delay line is employed to drive the amplifier inputs with digital waveforms directly. Efficiency benefits are realized. An analysis of harmonic termination impedance is conducted for each transistor output and related to total efficiency.

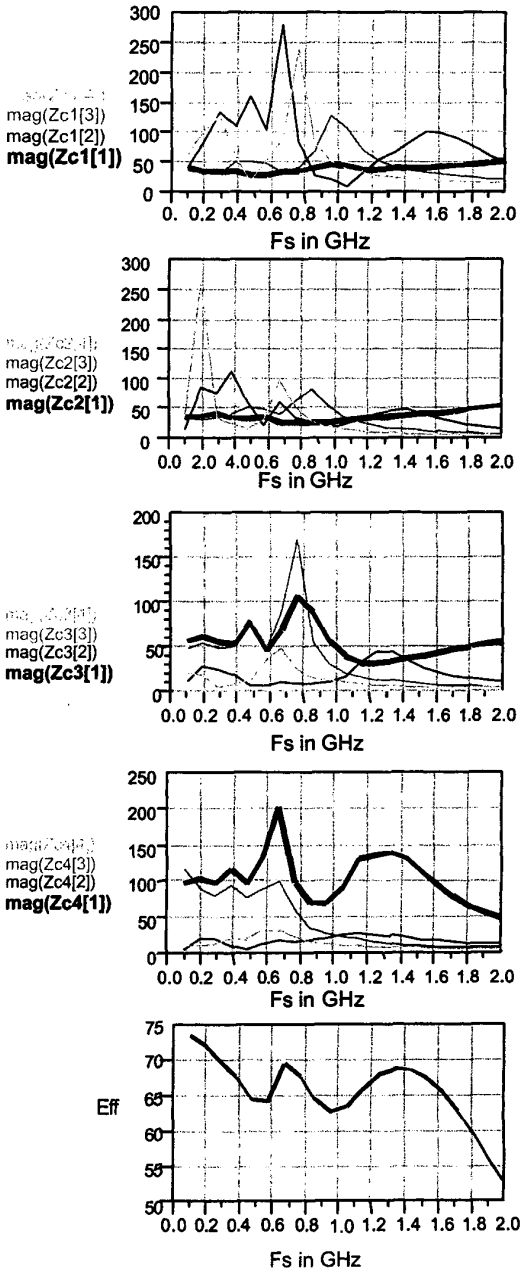
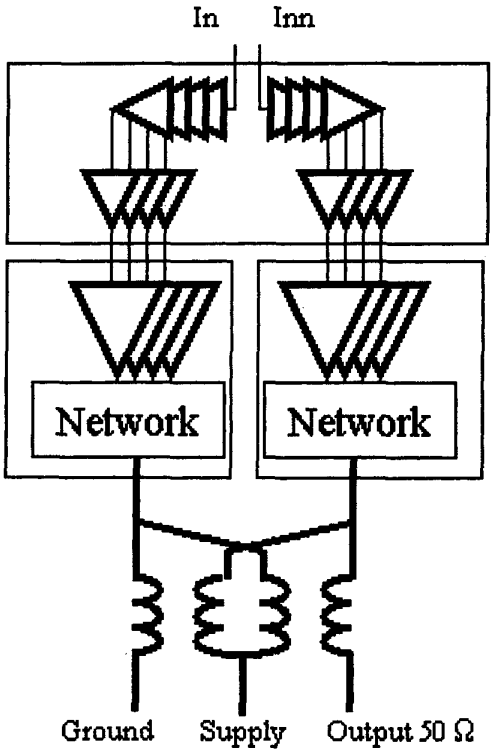


Fig. 5. Virtual Impedance of fundamental and first three harmonics at each collector node and total collector efficiency.

Fig. 6. Block diagram of the test fixture shown in Figure 7. The device supports single ended and differential distributed PA architectures.



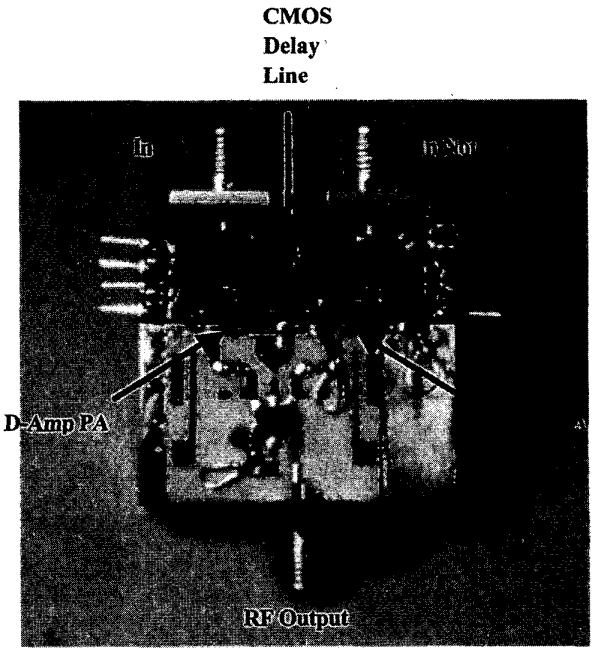


Fig. 7. Test fixture showing CMOS delay line and twin InGaP distributed power amplifiers in differential configuration of Figure 6.

ACKNOWLEDGEMENT

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REFERENCES

[1] W.R. Percival, "Improvements in and relating to thermionic valve circuits," British Patent No. 460 562 1936
[2] Internal Motorola report, B. Stengel, April 2000
[3] E. L. Ginzton, et al, "Distributed Amplification", IRE 1948